[0045] Conductor **218** also serves as the source and body conductor for the trench MOSFET portions of the device, shorting all the source regions **212** and body regions **204** together. The contact between the conductor **218** and the source and body regions **212**, **204** is an ohmic contact.

[0046] Titanium tungsten, platinum silicide, aluminum or a film containing two or more of these materials are some preferred materials for conductor **218** as they are capable of providing (a) a Schottky rectifying contact with the N-epitaxial region **202** and (b) an ohmic contact with both the source regions **212** and the body regions **204**.

[0047] Insulating regions **216**, typically silicon dioxide and/or BPSG (borophosphosilicate glass) regions, prevent the doped polycrystalline silicon regions **211** associated with the MOSFET gate function of the device from being shorted through the conductor **218** to the N+source regions **212** and the body regions **204**.

[0048] A conductor (not shown) is also typically provided adjacent the N+substrate **200**. This conductor acts both as the drain conductor for the MOSFET portions of the device and the cathode conductor for the Schottky diode portions. Another conductor (not shown) is also typically connected to a gate runner portion of the polycrystalline silicon **211** located outside of the active area of the device.

[0049] Hence, in the merged device of the present invention, both trench MOSFETs and Schottky diodes are integrated into the same piece of silicon. This design provides efficient use for the available surface area of the device. For example, as previously noted, the trench **219***b* containing the Schottky diode portion of the device shown in **FIG. 5** also has the feature that trench MOSFETs are incorporated into its sidewalls. In addition, this design further reduces costs by providing shared overhead (pads, perimeters, etc.) among the Schottky diode and trench MOSFET cells. Furthermore, the current in the device is relatively evenly distributed (leading, for example, to thermal advantage) with current flowing where desired (reducing, for example, inductive losses at high frequencies). This process further allows the Schottky diodes and the trench MOSFETs to the formed using common process steps in an integrated process scheme.

[0050] **FIGS. 6A** to **6**F illustrate a series of steps that can be performed to form the device depicted in **FIG. 5**. Referring now to **FIG. 6**A, an N-doped epitaxial layer **202** is first grown on a conventionally N+doped substrate **200**. Epitaxial layer can range, for example, from 1.3 to 25 microns in thickness. Next a body implant step is performed. For example, the upper surface of the epitaxial layer can be implanted with boron at 5 to 200 keV at a dosage of 10^{13} to $5\times10^{15}/cm^2$. Subsequently, an oxide layer **203** is formed over the surface, for example, by wet or dry oxidation at 800 to 1200° C. for 1 to 200 minutes. The oxide layer **203** can be, for example, from 500 to 10,000 Angstroms thick. In addition to forming oxide layer **203**, this step acts to diffuse the implanted dopant into the epitaxial layer **202** to form region **204**. In this case, the region **204** is a P-type region having a peak doping concentration of 10^{16} to 10^{20} cm^{-3} and a depth of 0.3 to 5.0 microns. The resulting structure is illustrated in **FIG. 6A**.

[0051] A source mask is then formed from oxide layer **203** by first providing a patterned photoresist layer (not shown) over layer **203**, followed by etching, for example using a wet or a plasma etching step, to remove the oxide in areas not covered by the photoresist. A source implant is then performed. For example, arsenic or phosphorous can be implanted at 5 to 200 keV and a dosage of 5×10^{14} to $1\times10^{16}/cm^2$. A wet or dry oxidation step is then performed, for example, at 800 to 1200° C. for 1 to 200 minutes, forming an oxide layer of 500 to 5000 Angstroms in thickness in the areas where the oxide was previously removed. This step also diffuses the source dopant, producing source regions **212** having a peak doping concentration of 10^{19} to 5×10^{20} cm^{-3} and a depth of 0.2 to 3.5 microns. The resulting structure is illustrated in **FIG. 6B**.

[0052] A trench mask (not shown) is then provided over the oxide layer **203**, after which trenches are etched, for example by plasma or reactive ion etching, to a depth typically ranging from 0.3 to 4.0 microns. This produces distinct P-body regions **204** and source regions **212**. The trench mask is then removed, and a sacrificial oxide layer is then grown and removed as is known in the art. Subsequently, a gate oxide layer **210**, ranging, for example, from 100 to 2000 Angstroms in thickness is grown within the trenches, for example, by wet or dry oxidation at 900 to 1200° C. for 1 to 60 minutes.

[0053] The surface of the structure is then covered, and the trenches are filled, with a polycrystalline silicon layer **211**, preferably using CVD. The polycrystalline silicon is typically doped N-type to reduce its resistivity. N-type doping can be carried out, for example, during CVD with phosphine gas, by thermal predeposition using phosphorous oxychloride, or by implantation with arsenic or phosphorous. The resulting structure is illustrated in **FIG. 6C**.

[0054] After appropriate masking outside of the active region to preserve polycrystalline silicon for gate contact, the polycrystalline silicon layer is then subjected to an anisotropic etching step, for example, a plasma or reactive ion etching step, forming distinct polycrystalline silicon regions **211**, which are connected within trenches that are out of the plane of the particular cross-section illustrated. The mask is then removed, and an oxide layer **216** is deposited, producing the structure illustrated in **FIG. 6D**.

[0055] A contact mask (i.e., a photoresist layer—not shown) is then provided, after which contact areas are opened in the oxide by an oxide etching step, consisting for example of a wet or plasma etch. This step provides contact areas corresponding to source/body contacts, Schottky rectifying contacts and gate contacts outside the active area. As with the polysilicon etch step, an anisotropic etch may be used to avoid the need for photoresist on the sloped polysilicon sidewalls in the center trench. The contact mask is then removed to produce the structure of **FIG. 6E**. If desired, P+regions (not shown) can be formed in upper portions of body regions **204**, using an additional mask, to establish a good ohmic contact with the conductor **218** that is subsequently provided. If sufficiently deep, these P+regions may also be formed around the perimeter of the Schottky diode. The resulting structure is shown in **FIG. 7**. It is also possible to form P+regions that just provide low resistance contacts to the body regions, or just provide p-doped regions that surround the Schottky diodes. In **FIG. 7**, the P+regions **220** provide both low resistance contacts and p-doped regions around the Schottky diodes, which increases breakdown.